ABSTRACT OF THE DISCLOSURE

An improved dual damascene structure is provided for use in the wiring-line structures of multi-level interconnects in integrated circuit. In this dual damascene structure, low-K (low dielectric constant) dielectric materials are used to form both the dielectric layers and the etch-stop layers between the metal interconnects in the IC device. With this feature, the dual damascene structure can prevent high parasite capacitance to occur therein that would otherwise cause large RC delay to the signals being transmitted through the metal interconnects and thus degrade the performance of the IC device. With the dual damascene structure, such parasite capacitance can be reduced, thus assuring the performance of the IC device.

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